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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MALKOWSKI, KENNETH J	
ART UNIT	**PAPER NUMBER**
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,302	FINISAR CORPORATION	
	Examiner	Art Unit	
	Kenneth J. Malkowski	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/28/03, 2/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0021468 to Kato et al. in view of U.S. Patent No. 6,075,634 to Casper et al.

With respect to claims 1 and 11-12, Kato discloses an integrated circuit for use in a transceiver module (integrated circuit having receiving and transmitting units, title), the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (t11 entering IC 110 at amplifier 141, Figure 3); receiver eye opener circuitry including components for retiming and reshaping the first serial electrical data stream (130, Figure 3 includes clock and data recovery circuit 132, Figure 2); a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (t22 exiting IC 120 into laser diode 41, Figure 3); a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (t21, t2C entering IC 120 at amplifier 142, Figure 3); a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (t12, t1C exiting at amplifier 140 in IC 110, Figure 3)(page 3 paragraph 38 (electrical data is serial electrical data)); and

loopback circuitry for switchably forming a loopback data path, the loopback data path comprising a loopback between a point on a receive path and a point on a transmit path, wherein the receive path is from the first electrical input port through the receiver eye opener circuitry to the first electrical output port and the transmit path is from the second electrical input port through the transmitter eye opener circuitry to the second electrical output port (170, Figure 3)(page 1 paragraph 11 (loopback path 170 is provided between transmitter and receiver portions of the integrated circuit)). However, Kato fails to disclose transmitter eye opener circuitry including components for retiming and reshaping the second serial electrical data stream. Despite this, transmitter eye opener circuitry is well known in the art. Casper, from the same field of endeavor discloses implementing a transmitter eye opener into the transmitting portion of a transceiver (columns 4-5 lines 61-67 and 1-10 (transmitter regenerator CDR unit removes amplitude noise, timing jitter creates regenerated serialized data stream))(21, Figure 1). Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to implement a transmitter eye opener as taught by Casper into the transmit portion of the transceiver as taught by Kato. The motivation for doing so would have been to both pre and post-compensate for distortion and timing jitter to ensure accurate regeneration of the data at the receive end of the extended link (Casper: column 6 lines 29-51).

With respect to claims 2-8 Kato in view of Casper disclose the integrated circuit of claim 1 (Kato: 10, Figure 3) wherein the loopback data path (Kato: 170, Figure 3) is from the first electrical input port (Kato: t11 entering IC 110 at amplifier 141, Figure 3) to

the first electrical output port (Kato: t22 exiting IC 120 into laser diode 41, Figure 3). Another loop-back implementation disclosed is from the second electrical output to the second electrical input (170, Figure 1B). It is important to note that the loopback as taught by Kato in view of Casper could have a multitude of configurations all of which are designed to produce feedback between transmitter and receiver IC circuits. Therefore, the various implementations of loopback paths discussed in claims 2-9 are obvious variations in design choice in that it is well known to one of ordinary skill in the art that loopback paths can include a various array of elements for various feedback purposes depending on the intent of the designer. Kato suggests that the loopback path may include various different components as the result of different design choices (Kato: page 4 paragraph 58 (loop back path may include data information, clock information or both)).

With respect to claim 9, Kato in view of Casper disclose the integrated circuit of claim 1 further comprising: loopback control circuitry coupled to the loopback circuitry for controlling the loopback circuitry to form the loopback data path (Buffer IC, 60 Figure 1B)(page 1 paragraph 11).

With respect to claim 10, Kato in view of Casper disclose the integrated circuit of claim 1, however fail to disclose power management circuitry for powering down the loopback circuitry when the loopback data path is not formed. Despite this, power management circuitry that shuts off circuitry that is not being used was extremely well known in the art at the time of invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize power management circuitry

in the integrated circuit as taught by Kato in view of Casper. The motivation for doing so would have been to save on operation cost by only using power when necessary.

3. Claims 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0021468 to Kato et al. in view of U.S. Patent No. 6,075,634 to Casper et al. and further in view of U.S. Patent Application Publication No. 2002/0149812 to Hong et al.

With respect to claims 13, 23 and 26 Kato discloses an integrated circuit for use in a transceiver module (integrated circuit having receiving and transmitting units, title), the integrated circuit comprising: a first electrical input port for receiving a first serial electrical data stream (t11 entering IC 110 at amplifier 141, Figure 3); receiver eye opener circuitry including components for retiming and reshaping the first serial electrical data stream (130, Figure 3 includes clock and data recovery circuit 132, Figure 2); a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit (t22 exiting IC 120 into laser diode 41, Figure 3); a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit (t21, t2C entering IC 120 at amplifier 142, Figure 3); a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream (t12, t1C exiting at amplifier 140 in IC 110, Figure 3)(page 3 paragraph 38 (electrical data is serial electrical data)); However, Kato fails to disclose transmitter eye opener circuitry including components for retiming and reshaping the second serial electrical data stream. Despite this, transmitter eye opener circuitry is well known in the art. Casper, from the same field of endeavor

discloses implementing a transmitter eye opener into the transmitting portion of a transceiver (columns 4-5 lines 61-67 and 1-10 (transmitter regenerator CDR unit removes amplitude noise, timing jitter creates regenerated serialized data stream))(21, Figure 1). Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to implement a transmitter eye opener as taught by Casper into the transmit portion of the transceiver as taught by Kato. The motivation for doing so would have been to both pre and post-compensate for distortion and timing jitter to ensure accurate regeneration of the data at the receive end of the extended link (Casper: column 6 lines 29-51).

Furthermore, Kato in view of Casper fail to disclose a bit error rate tester (BERT) engine for testing a test data path. Despite this, BERT engines are well known in the art as an advantageous implementation for optical communication devices. Hong, from the same field of endeavor discloses a bit error rate tester (BERT) engine (page 2 paragraphs 22-23 (BERT)) for testing a test data path from a starting test point to an ending test point (path from transmitter 18 to receiver 30, figure 1), the starting test point and the ending test point each located on either a receive path or on a transmit path (page 2 paragraph 23). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the BERT as taught by Hong into the transmit/receive path in the transceiver as taught by Kato in view of Casper. The motivation for doing so would have been to investigate the quality and performance of an optical network (Hong: page 2 paragraph 16).

With respect to claims 14-19, Kato in view of Casper and further in view of Hong disclose the integrated circuit of claim 13, however do not disclose each and every various design implementation detailed in claims 14-18. It is important to note that the bit error rate testing as taught by Kato in view of Casper and further in view of Hong could have a multitude of configurations all of which are designed to investigate signal quality within a signaling network. Therefore, the various implementations of bit error rate testing discussed in claims 14-18 are obvious variations in design choice in that it is well known to one of ordinary skill in the art that bit error rate testing can include a various array of elements for various testing purposes depending on the intent of the designer. Hong teaches that it is important to examine several different components/ factors which could contribute to bit error in an optical system (page 2 paragraph 16) by isolating each penalty contributing factor. With specific reference to claim 19, Hong also teaches that it is well known to those of ordinary skill in the art that any number of various test patterns may be applied during the testing and that the invention is not limited to a particular test pattern or testing protocol (page 3 paragraph 25).

With respect to claim 20, Kato in view of Casper and further in view of Hong disclose the integrated circuit of claim 13 wherein the BERT engine comprises: pattern generator circuitry coupled to the starting test point, for generating a test pattern for testing the test data path (page 3 paragraph 25 (test pattern))(40, Figure 2)(28, Figure 1); and error detector circuitry coupled to the ending test point, for detecting errors in the test pattern (page 2 paragraph 22 (calculate BER))(16, Figure 1).

With respect to claim 21, Kato in view of Casper and further in view of Hong disclose the integrated circuit of claim 13 further comprising: BERT control circuitry coupled to the BERT engine for controlling testing of the test data path (pages 1-2 paragraphs 12-13).

With respect to claim 22, Kato in view of Casper and further in view of Hong disclose the integrated circuit of claim 13, however fails to disclose power management circuitry for powering down the BERT engine when no testing of the test data path is occurring. Despite this, power management circuitry that shuts off circuitry that is not being used was extremely well known in the art at the time of invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize power management circuitry in the integrated circuit as taught by Kato in view of Casper. The motivation for doing so would have been to save on operation cost by only using power when necessary.

With respect to claim 24, Kato in view of Casper and further in view of Hong disclose the method of claim 23, however do not specifically disclose wherein the test pattern has a data rate of at least approximately 10 Gb/s. Despite this, it is clear that any specific rate could be used to transmit the test pattern, including 10 Gb/s. It is further clear that deciding on a specific rate for a test pattern, including 10 Gb/s would have been obvious as a mere matter of design choice at the time of invention. Furthermore, Hong teaches that that it is well known to those of ordinary skill in the art that any number of various test patterns may be applied during the testing and that the

invention is not limited to a particular test pattern or testing protocol (page 3 paragraph 25).

With respect to claim 25, Kato in view of Casper and further in view of Hong disclose the method of claim 23 further comprising: detecting errors in the test pattern received at the ending test point (Hong: page 2 paragraph 22 (received channels may be processed by a BERT module in order to calculate BER)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth J. Malkowski whose telephone number is (571) 272-5505. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

6/10/07

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER